GENERAL DESCRIPTION

CM6500UN is a ZVS-Like Single PFC and it is designed to meet EPA 90+ spec. (total efficiency). It has the following key features.

1.) Around 2% efficiency gain when the output load is below 60% of the full load

2.) High Voltage 420V bulk capacitor can be reduced, and also PFC Boost Capacitor ripple current can be reduced

3.) Turbo Speed PFC may reduce 420 Bulk Capacitor size further

4.) A PGB function is designed for interfacing to next stage controller or the House Keeping IC at secondary side. The PGB function pull low was decide by IC inside. The PGB Pull high It has a customer programmable by PGTHL low threshold.

5.) "Remember it was Light Load" function and "Remember it was Full Load" function may reduce PFC 420V Bulk Capacitor size further. It boosts the total efficiency as well.

6.) IAC, Vrms, VFB pin resistor can be use > 5M ohm. It will help No Load Consumption to reduce at 270VAC

7.) Better Power Factor and Better THD

8.) Clean Digital PFC Brown Out

9.) Dynamic Soft PFC to ease the stress over the entire external power device is reduced and EMI noise reduced

10.) Superior Surge Noise Immunity

CM6500UN is designed to meet the EPA/90+ regulation. With the proper design, its efficiency of power supply can easily approach 90+/92+.

FEATURES

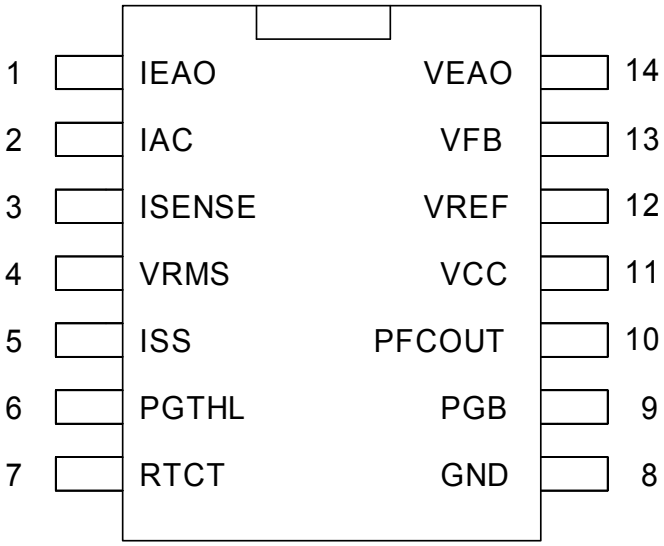
- Patents Pending
- 23V Bi-CMOS process.
- Designed for EPA/90+efficiency
- Customer Programmable the Low Threshold of PGB comparator at PGTHL pin
- "Remember It was Light Load" function to improve the efficiency and Hold up Time
- "Remember It was Full Load" function to improve the efficiency and Hold up Time
- Clean Digital PFC Brown Out
- All high voltage resistors can be greater than 5 Mega ohm (5 Mega to 8 Mega ohm) to improve the no load consumption.
- Rail to rail CMOS Drivers with on, 24 ohm and off, 12 ohm with 17V zeners.
- Fast Start-UP Circuit without extra bleed resistor to aid VCC reaches 13V sooner.
- Low start-up current (50uA typ.)
- Low operating current (2.1mA typ.)
- Adjustable Long Delay Time for Line Sagging (Up to 2 Second)
- 17V VCC shunt regulator
- Dynamic Soft PFC to ease the stress of the Power Device and Ease the EMI-filter design.
- Better Power Factor and Better THD
- Average current mode control, continuous or discontinuous boost leading edge PFC.
- Current fed Gain Modulator for improved noise immunity.
- Gain Modulator is a constant maximum power limiter.
- Precision Current Limit, over-voltage protection, UVLO, and soft start, and Reference OK.

APPLICATIONS

- EPA/90+ related Power Supply
- Desktop PC Power Supply
- Internet Server Power Supply
- LCD Power Supply
- PDP Power Supply
- AC Adaptor
- IPC Power Supply
- UPS
- Battery Charger
- DC Motor Power Supply
- Monitor Power Supply
- Telecom System Power Supply
- Distributed Power

PIN CONFIGURATION

SOP-14 & DIP-14
TOP View

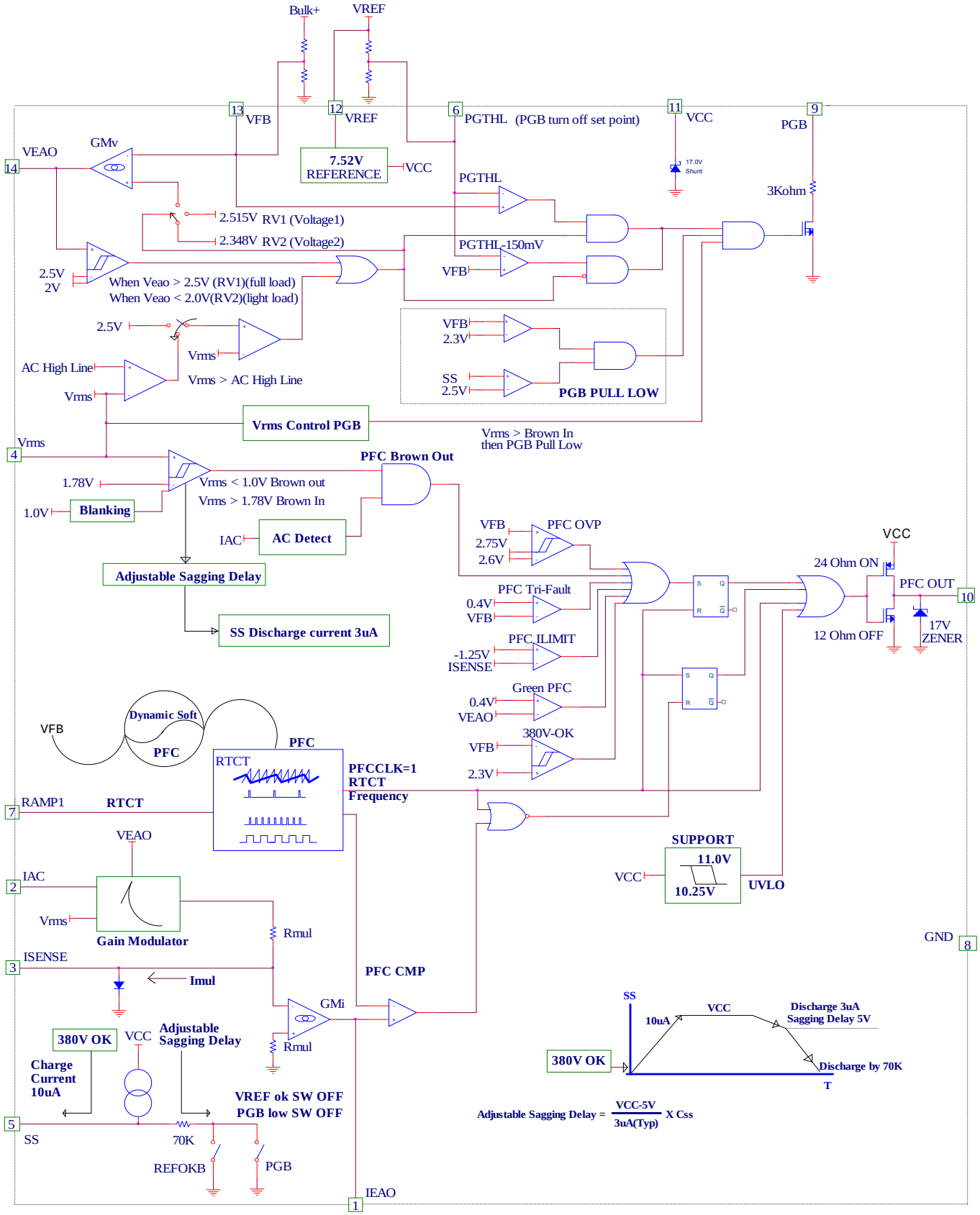


PIN DESCRIPTION

Pin No.	Symbol	Description	Operating Voltage			
			Min.	Typ.	Max.	Unit
1	I_{EAO}	PFC transconductance current error amplifier output **(GMi).**	0		VREF	V
2	I_{AC}	IAC has 2 functions: 1. PFC gain modulator reference input. 2. Typical RAC resistor is about 6 Mega ohm to 8 Mega ohm to sense the line.	0		100	uA
3	I_{SENSE}	PFC Current Sense: for both Gain Modulator and PFC current ILIMIT comparator.	-1.3		0.7	V
4	V_{RMS}	Line Input Sense pin for multiplier and also it is the PFC Brown out sense pin.	0		6	V
5	ISS	1)PFC Soft Start pin: It supplies ~ 10uA to SS pin. It provides a close-loop soft start function during power supply start up. PFC Soft Start function can adjust by a simple capacitor to ground and it can be around 1uF. 2)When AC turn off VFB voltage sense is lower than PGTHL(PGB comparator), SS pin is discharged through an internal ~ 70K Ohm resistor.	0		VCC	V

6	**PGTHL**	PGTHL is an input I/O. The user can program the Low Threshold of the Power Good which can determine the comparator output of PGB (open drain) to be pulled high.	0		VREF	V
7	**RTCT**	Oscillator timing node; timing set by RT and CT	0.8		4	V
8	**GND**	Ground				
9	**PGB**	PGB is the PG comparator output. The input of PG comparator is using Vfb (pin 13) to compare with the high threshold 2.25V (preset internally) and the low threshold comparator with PGTHL (pin 6, Set up by user). When Bulk Voltage 380V is ready, pin 9 is open-drain and it will be pulled low. When Bulk Voltage Drop (VFB=PGTHL) set up point it will be pulled high.	0		VCC	V
10	**PFC OUT**	PFC driver output	0		VCC	V
11	**V_{CC}**	Positive supply for CM6500UN **Note : Vcc must keep 11.5V(U.V.L.O high) or above for the sufficient turn on voltage**	10	15	20	V
12	**VREF**	Maximum 3.5mA buffered output for the internal 7.5V reference when VCC=14V		7.5		V
13	**V_{FB}**	PFC transconductance voltage error amplifier input	0	2.5	3	V
14	**VEAO**	PFC transconductance voltage error amplifier output (GMv)	0		6	V

SIMPLIFIED BLOCK DIAGRAM (CM6500UN)



ORDERING INFORMATION

Part Number	Temperature Range	Package
CM6500UNXIS*	-40℃ to 125℃	14-Pin SOP (S14)
CM6500UNXISTR*	-40℃ to 125℃	14-Pin SOP (S14)
CM6500UNXIP*	-40℃ to 125℃	14-Pin DIP (P14)

***Note:** X : Suffix for Halogen Free and PB Free Product
TR : Package is Tape & Reel

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are those values beyond which the device could be permanently damaged.

Parameter	Min.	Max.	Units
V_{CC}		21	V
VREF	GND – 0.3	8	V
VREF (transient/load regulation) overshoot (period less than 1ms)		8.5	V
VREF (transient/load regulation) overshoot (period less than 300us)		10	V
IEAO/VEAO/Vrms/RTCT/PGTHL	GND – 0.3	VREF+0.3	V
IAC/PGB/SS	GND – 0.3	VCC+0.7	V
VFB	GND – 0.3	5	V
I_{SENSE} Voltage	-5	0.7	V
I_{SENSE} Voltage (period less than 1ms)	-10	0.7	V
PFC OUT	GND – 0.3	VCC + 0.3	V
PFC Out Driver (period less than 50ns)	GND – 3.0	VCC + 0.3	V
PFC Out Driver (period less than 25ns)	GND – 5.0	VCC + 0.3	V
Peak PFC OUT Current, Source or Sink		0.5	A
Peak PFC OUT Current, Source or Sink (period less than 5us)		1	A
PFC OUT, Energy Per Cycle		1.5	μJ
I_{REF}		3.5	mA
I_{AC} Input Current		1	mA
Junction Temperature		150	℃
Storage Temperature Range	-65	150	℃
Operating Temperature Range	-40	125	℃
Lead Temperature (Soldering, 10 sec)		260	℃
Thermal Resistance (θ_{JA}) Plastic DIP Plastic SOIC		 80 105	 ℃/W ℃/W

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply Vcc=+14V, PGTHL=+2.0V, R_T = 27kΩ, C_T = 1000pF, T_A=Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6500UN			Unit
			Min.	Typ.	Max.	
Clean Digital PFC Brown in/Out						
	VRMS Threshold High	Room Temperature=25℃	1.71	1.78	1.80	V
	VRMS Threshold Low	Room Temperature=25℃	0.98	1.02	1.06	V
	Hysteresis		750	760	790	mV
Voltage Error Amplifier (GMv) VEAO						
	Input Voltage Range		0		6	V
	Transconductance	V_{NONINV} = V_{INV}, VEAO = 2.25V @ T=25℃	30	40	50	μmho
VFB(high) **Full load**	Feedback Reference Voltage	Vrms > AC High Line Threshold Veao > 2.5V and Vrms < AC high Line Threshold	2.49	2.515	2.54	V
Light/Full Load determine (Veao Threshold)						
	Output High Voltage		5.8	6.0		V
	Output Low Voltage			0.1	0.4	V
	Source Current	Overdrive Voltage = 100mV @ T=25℃	1	3	5	μA
	Sink Current	Overdrive Voltage = 100mV @ T=25℃	-45		-25	μA
	Open Loop Gain	DC gain	30	40		dB
	Power Supply Rejection Ratio	11V < V_{CC} < 16.5V	60	75		dB
Current Error Amplifier (GMi) IEAO						
	Transconductance	V_{NONINV} = V_{INV}, IEAO = 1.5V @ T=25℃	60	70	80	μmho
	Input Offset Voltage	VEAO=0V, IAC is open	-12		12	mV
	Output High Voltage		6.8	7.3	7.8	V
	Output Low Voltage			0.1	0.4	V

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, these specifications apply Vcc=+14V, PGTHL=+2.0V, R_T = 27kΩ, C_T = 1000pF, T_A=Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6500UN			Unit
			Min.	Typ.	Max.	
	Sink Current	I_{SENSE} = -0.5V, IEAO = 1.5V	-45	-35	-25	μA
	Source Current	I_{SENSE} = +0.5V, IEAO = 4.0V	25	35	45	μA
	Open Loop Gain	DC Gain	30	40		dB
	Power Supply Rejection Ratio	11V < V_{CC} < 16.5V	60	75		dB
PFC OVP Comparator						
	Threshold Voltage		2.65	2.75	2.85	V
	Hysteresis		140		240	mV
PFC Green Power Detect Comparator						
	Veao Threshold Voltage		0.3	0.4	0.5	V
Tri-Fault Detect						
	Fault Detect HIGH		2.65	2.75	2.85	V
	Time to Fault Detect HIGH	V_{FB}=$V_{FAULT\ DETECT\ LOW}$ to V_{FB}=OPEN, 470pF from V_{FB} to GND		2	4	ms
	Fault Detect LOW		0.3	0.4	0.5	V
PFC I_{LIMIT} Comparator(PFC current limit)						
	Threshold Voltage		-1.375	-1.25	-1.125	V
	($PFCI_{LIMIT}$– Gain Modulator Output)		300	450		mV
	Delay to Output (Note 4)			700		ns
PGTHL(set up PGB pull high;turn off point)						
	PGB_CMP_LOW	Sweep VFB than check PGB CMP pull low	2.1		2.3	
	PGB_CMP_HIGH	Setup Vref 分壓, PGTHL=2V, VEAO=3V Sweep VFB Voltage Check PGB CMP Pull-High	1.949		2.035	V
	Remember (Full Load) – (Light Load) Hysteresis		130	150	170	mV

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply Vcc=+14V, PGTHL=+2.0V, R_T = 27kΩ, C_T = 1000pF, T_A=Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6500UN			Unit
			Min.	Typ.	Max.	
GAIN Modulator						
	Gain1 (Note 3)	I_{AC} = 20 μA, V_{RMS} =1.125, V_{FB} = 2.375V @ T=25℃	5	6	7.2	
	Gain2 (Note 3)	I_{AC} = 20 μA, V_{RMS} = 1.45588V, V_{FB} = 2.375V @ T=25℃	4	5	6	
	Gain3 (Note 3)	I_{AC} = 20 μA, V_{RMS} =2.91V, V_{FB} = 2.375V @ T=25℃	1.2	1.4	1.6	
	Gain4 (Note 3)	I_{AC} = 20 μA, V_{RMS} = 3.44V, V_{FB} = 2.375V @ T=25℃	0.8	1	1.2	
	Bandwidth (Note 4)	I_{AC} = 40 μA		1		MHz
	Output Voltage = Rmul * (I_{SENSE}-I_{OFFSET})	I_{AC} = 50 μA, V_{RMS} = 1.125V, V_{FB} = 2.375V VEAO=6V	0.7	0.8	0.9	V
	I(V)mul Threshold (low)	VEAO=2V	0.3		0.365	V
Oscillator (Measuring fpfc)						
	Initial fpfc Accuracy 1	R_T = 27 kΩ, C_T = 1000pF, T_A = 25℃ IAC=0uA	60	66	72	kHz
	Voltage Stability	11V < V_{CC} < 16.5V		2		%
	Temperature Stability			2		%
	Ramp Valley to Peak Voltage	VEAO=6V and IAC=20uA		2.5		V
	PFC Dead Time (Note 4)		600		1000	ns
	CT Discharge Current	V_{RAMP2} = 0V, V_{RAMP1} = 2.5V	9	10	11	mA

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply Vcc=+14V, PGTHL=+2.0V, R_T = 27kΩ, C_T = 1000pF, T_A=Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6500UN			Unit
			Min.	Typ.	Max.	
Reference						
	Output Voltage	T_A = 25℃, I(VREF) = 0mA	7.48	7.52	7.56	V
	Line Regulation	11V < V_{CC} < 16.5V@ T=25℃		3	8	mV
	Load Regulation	VCC=10.5V,0mA < I(VREF) < 2.0mA; @ T=25℃		25	50	mV
		VCC=14V,0mA < I(VREF) < 3.5mA; T_A = -40℃~85℃		25	50	mV
	Temperature Stability			0.4		%
	Total Variation	Line, Load, Temp	7.3		7.7	V
	Long Term Stability	T_J = 125℃, 1000HRs	5		25	mV
PFC						
	Minimum Duty Cycle	V_{IEAO} > 4.5V		0		%
	Maximum Duty Cycle	V_{IEAO} < 1.2V	93	95		%
	Output Low Rdson	I_{OUT} = -20mA @ T=25℃		12	18	ohm
		I_{OUT} = -100mA @ T=25℃			18	ohm
		I_{OUT} = 10mA, V_{CC} = 9V @ T=25℃		0.5	1	V
	Output High Rdson	I_{OUT} = 20mA @ T=25℃		24	40	ohm
		I_{OUT} = 100mA @ T=25℃			40	ohm
	Rise/Fall Time (Note 4)	C_L = 100pF @ T=25℃		50		ns
Soft Start						
	Soft Start Current	Room Temperature=25℃	7	10	12	μA
	Soft Start Discharge Current	Vrms=brown out, Soft Start=VCC to 5V	1	3	5	μA
Supply						
	Start-Up Current	V_{CC} = 12V, C_L = 0 @ T=25℃		50	75	uA
	Operating Current	14V, C_L = 0		2.5	3.5	mA
Turn-On	Under voltage Lockout Threshold	CM6500UN	10.5	11	11.5	V
Turn-Off	Under voltage Lockout Hysteresis	CM6500UN		0.75	1.1	V
Shunt Regulator (VCC zener)						
	Zener Threshold Voltage	Apply VCC with Iop=20mA	16.5	17	17.5	V

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Includes all bias currents to other circuits connected to the V_{FB} pin.

Note 3: Gain ~ K x 5.3V; K = (I_{SENSE} – I_{OFFSET}) x [I_{AC} (VEAO – 0.7)]$^{-1}$; $VEAO_{MAX}$ = 6V

Note 4: Guaranteed by design, not 100% production test.

Getting Start

To start evaluating CM6500UN from the exiting CM6502 , need to be taken care before doing the fine tune:

1.) Change RTCT pin (pin 7) from the existing value to RT=27K ohm and CT=1000pF to have fpfc = fRTCT = 68Khz for CM6500UN.
2.) Adjust all high voltage resistor around 5 mega ohm or higher first.
3.) VRMS pin (pin 4) needs to be 1.1V at VIN=80Vac right before PFC brown out and to be 1.78V at VIN=85VAC right before PFC brown in for universal input application for line input from 85VAC to 270VAC.
5.) At full load, the average Veao needs to be around 4.2V and the ripple on the Veao needs to be less than 300mV when the light load comparator are triggered.

Functional Description

CM6500UN is designed for high efficient power supply for both full load and light load. It is a ZVS-Like PFC supply controller.

The CM6500UN is an average current controlled, continuous/discontinuous boost Power Factor Correction (PFC) which uses leading edge modulation.

In addition to power factor correction, a number of protection features have been built into the CM6500UN. These include soft-start, PFC over-voltage protection, peak current limiting, brownout protection, duty cycle limiting, and under-voltage lockout.

Power Factor Correction

Power factor correction makes a nonlinear load look like a resistive load to the AC line. For a resistor, the current drawn from the line is in phase with and proportional to the line voltage, so the power factor is unity (one). A common class of nonlinear load is the input of most power supplies, which use a bridge rectifier and capacitive input filter fed from the line. The peak-charging effect, which occurs on the input filter capacitor in these supplies, causes brief high-amplitude pulses of current to flow from the power line, rather than a sinusoidal current in phase with the line voltage. Such supplies present a power factor to the line of less than one (i.e. they cause significant current harmonics of the power line frequency to appear at their input). If the input current drawn by such a supply (or any other nonlinear load) can be made to follow the input voltage in instantaneous amplitude, it will appear resistive to the AC line and a unity power factor will be achieved.

To hold the input current draw of a device drawing power from the AC line in phase with and proportional to the input voltage, a way must be found to prevent that device from loading the line except in proportion to the instantaneous line voltage. The PFC section of the CM6500UN uses a boost-mode DC-DC converter to accomplish this. The input to the converter is the full wave rectified AC line voltage. No bulk filtering is applied following the bridge rectifier, so the input voltage to the boost converter ranges (at twice line frequency) from zero volts to the peak value of the AC input and back to zero. By forcing the boost converter to meet two simultaneous conditions, it is possible to ensure that the current drawn from the power line is proportional to the input line voltage. One of these conditions is that the output voltage of the boost converter must be set higher than the peak value of the line voltage. A commonly used value is 385VDC, to allow for a high line of $270VAC_{rms}$. The other condition is that the current drawn from the line at any given instant must be proportional to the line voltage. Establishing a suitable voltage control loop for the converter, which in turn drives a current error amplifier and switching output driver satisfies the first of these requirements. The second requirement is met by using the rectified AC line voltage to modulate the output of the voltage control loop. Such modulation causes the current error amplifier to command a power stage current that varies directly with the input voltage. In order to prevent ripple, which will necessarily appear at the output of boost circuit (typically about 10VAC on a 385V DC level); from introducing distortion back through the voltage error amplifier, the bandwidth of the voltage loop is deliberately kept low. A final refinement is to adjust the overall gain of the PFC such to be proportional to 1/(Vin x Vin), which linearizes the transfer function of the system as the AC input to voltage varies.

Since the boost converter topology in the CM6500UN PFC is of the current-averaging type, no slope compensation is required.

More exactly, the output current of the gain modulator is given by:

Dynamic Soft PFC (patent pending)

Dynamic Soft PFC is the main feature of CM6500UN. Dynamic Soft PFC is to improve the efficiency, to reduce power device stress, to ease EMI, and to ease the monotonic output design while it has the more protection such as the short circuit with power-fold-back protection. Its unique sequential control maximizes the performance and the protections among steady state, transient and the power on/off conditions.

PFC Section:

Gain Modulator

Figure 1 shows a block diagram of the PFC section of the CM6500UN. The gain modulator is the heart of the PFC, as it is this circuit block which controls the response of the current loop to line voltage waveform and frequency, rms line voltage, and PFC output voltages. There are three inputs to the gain modulator. These are:

1. A current representing the instantaneous input voltage (amplitude and wave-shape) to the PFC. The rectified AC input sine wave is converted to a proportional current via a resistor and is then fed into the gain modulator at I_{AC}. Sampling current in this way minimizes ground noise, as is required in high power switching power conversion environments. The gain modulator responds linearly to this current.
2. A voltage proportional to the long-term RMS AC line voltage, derived from the rectified line voltage after scaling and filtering. This signal is presented to the gain modulator at VRMS. The gain modulator's output is inversely proportional to V_{RMS}^2. The relationship between V_{RMS} and gain is illustrated in the Typical Performance Characteristics of this page.
3. The output of the voltage error amplifier, VEAO. The gain modulator responds linearly to variations in this voltage.

The output of the gain modulator is a current signal, in the form of a full wave rectified sinusoid at twice the line frequency. This current is applied to the virtual-ground (negative) input of the current error amplifier. In this way the gain modulator forms the reference for the current error loop, and ultimately controls the instantaneous current draw of the PFC from the power line. The general formula of the output of the gain modulator is:

$$I_{mul} = \frac{I_{AC} \times (VEAO - 0.7V)}{V_{RMS}^2} \text{ x constant} \qquad (1)$$

Gain=Imul/Iac

K=Gain/(VEAO-0.7V)

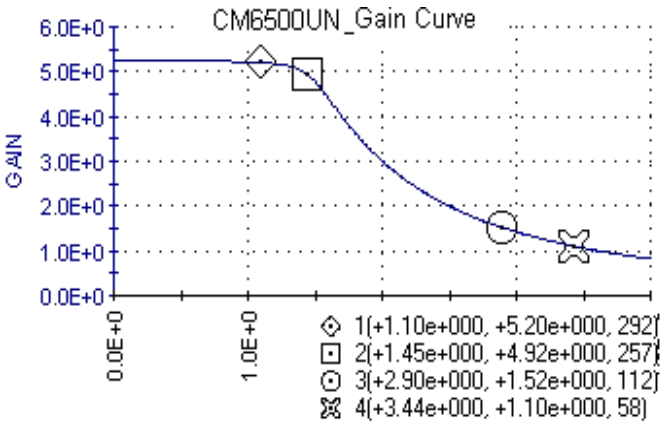
$I_{mul} = K \times (VEAO - 0.7V) \times I_{AC}$

Where K is in units of [V^{-1}]

Note that the output current of the gain modulator is limited around 140μA and the maximum output voltage of the gain modulator is limited to 140uA x 5.7K=0.8V. This 0.8V also will determine the maximum input power.

However, $I_{GAINMOD}$ cannot be measured directly from I_{SENSE}. I_{SENSE} = $I_{GAINMOD}$-I_{OFFSET} and I_{OFFSET} can only be measured when VEAO is less than 0.5V and $I_{GAINMOD}$ is 0A. Typical I_{OFFSET} is around 25uA.

IAC=20uA, VEAO=6V



Gain vs. VRMS (pin4)

When VRMS below 1V, the PFC is shut off. Designer needs to design 80VAC with VRMS average voltage= 1.14V.

$$\text{Gain} = \frac{I_{SENSE} - I_{OFFSET}}{I_{AC}} = \frac{I_{MUL}}{I_{AC}}$$

Selecting R_{AC} for IAC pin

IAC pin is the input of the gain modulator. IAC also is a current mirror input and it requires current input. By selecting a proper resistor R_{AC}, it will provide a good sine wave current derived from the line voltage and it also helps program the maximum input power and minimum input line voltage.

R_{AC}=Vin min peak x 50K. For example, if the minimum line voltage is 85VAC, the R_{AC}=85 x 1.414 x 50K = 6.0 Mega ohm.

VRMS Description

VRMS pin is designed for the following functions:

1. VRMS is used to detect the AC Brown Out (Also, we can call it Clean Digital PFC brown out.). When VRMS is less than 1.03 V +/-5%, PFCOUT will be turned off and VEAO will be softly discharged. When VRMS is greater than 1.78V +/-5%, PFCOUT is enabled and VEAO is released.

Current Error Amplifier, IEAO

The current error amplifier's output controls the PFC duty cycle to keep the average current through the boost inductor a linear function of the line voltage. At the inverting input to the current error amplifier, the output current of the gain modulator is summed with a current which results from a negative voltage being impressed upon the I_{SENSE} pin. The negative voltage on I_{SENSE} represents the sum of all currents flowing in the PFC circuit, and is typically derived from a current sense resistor in series with the negative terminal of the input bridge rectifier.

In higher power applications, two current transformers are sometimes used, one to monitor the IF of the boost diode. As stated above, the inverting input of the current error amplifier is a virtual ground. Given this fact, and the arrangement of the duty cycle modulator polarities internal to the PFC, an increase in positive current from the gain modulator will cause the output stage to increase its duty cycle until the voltage on I_{SENSE} is adequately negative to cancel this increased current. Similarly, if the gain modulator's output decreases, the output duty cycle will decrease, to achieve a less negative voltage on the I_{SENSE} pin.

Error Amplifier Compensation

The PWM loading of the PFC can be modeled as a negative resistor; an increase in input voltage to the PWM causes a decrease in the input current. This response dictates the proper compensation of the two transconductance error amplifiers. Figure 2 shows the types of compensation networks most commonly used for the voltage and current error amplifiers, along with their respective return points. The current loop compensation is returned to V_{REF} to produce a soft-start characteristic on the PFC: as the reference voltage comes up from zero volts, it creates a differentiated voltage on I_{EAO} which prevents the PFC from immediately demanding a full duty cycle on its boost converter.

Clean Digital PFC Brown Out

Clean Digital PFC Brown Out provides a clean cut off when AC input is much lower than regular AC input voltage such as 67Vac.

Inside of Clean Digital PFC Brown Out, there is a comparator monitors the VRMS (pin 4) voltage. Clean Digital PFC Brown Out inhibits the PFC and VEAO (PFC error amplifier output) is pulled down when the VRMS is lower than off threshold, 1.04V (The off Vin voltage usually corresponds to 70Vac). When the VRMS voltage reaches 1.75V (The On Vin voltage usually corresponds to 86.62V and when Vin = 80Vac, VRMS = 1.14V), PFC is on.

Before PFC is turned on, VRMS (pin 4) represents the peak voltage of the AC input. Before PFC is turned off, VRMS (pin 4) represents the VRMS voltage of the AC input.

Cycle-By-Cycle Current Limiter and Selecting R_{SENSE}

The I_{SENSE} pin, as well as being a part of the current feedback loop, is a direct input to the cycle-by-cycle current limiter for the PFC section. Should the input voltage at this pin ever be more negative than –1.3V, the output of the PFC will be disabled until the protection flip-flop is reset by the clock pulse at the start of the next PFC power cycle.

R_S is the sensing resistor of the PFC boost converter. During the steady state, line input current x R_{SENSE} = I_{mul} x 5.7K. Since the maximum output voltage of the gain modulator is I_{mul} max x 5.7K= 0.8V during the steady state, R_{SENSE} x line input current will be limited below 0.8V as well. When VEAO reaches maximum VEAO which is 6V, Isense can reach -0.8V. At 100% load, VEAO should be around 4.5V and ISENSE average peak is -0.6V. It will provide the optimal dynamic response + tolerance of the components.

Therefore, to choose R_{SENSE}, we use the following equation:

R_{SENSE} + $R_{Parasitic}$ =0.6V x Vinpeak / (2 x Line Input power)

For example, if the minimum input voltage is 80VAC, and the maximum input rms power is 200Watt, R_{SENSE} + $R_{Parasitic}$ = (0.6V x 80V x 1.414) / (2 x 200) = 0.169 ohm. The designer needs to consider the parasitic resistance and the margin of the power supply and dynamic response. Assume $R_{Parasitic}$ = 30 mOhm, R_{SENSE} = 139 mOhm.

PFC OVP

In the CM6500UN, PFC OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load should suddenly change. A resistor divider from the high voltage DC output of the PFC is fed to VFB. When the voltage on VFB exceeds 2.79V, the PFC output driver is shut down. The PWM section will continue to operate. The OVP comparator has 250mV of hysteresis, and the PFC will not restart until the voltage at VFB drops below 2.54V. The VFB power components and the CM6500UN are within their safe operating voltages, but not so low as to interfere with the boost voltage regulation loop.

PFC Voltage Loop

There are two major concerns when compensating the voltage loop error amplifier, V_{EAO}; stability and transient response. Optimizing interaction between transient response and stability requires that the error amplifier's open-loop crossover frequency should be 1/2 that of the line frequency, or 23Hz for a 47Hz line (lowest anticipated international power frequency).

deviate from its 2.5V (nominal) value. If this happens, the transconductance of the voltage error amplifier, GMv will increase significantly, as shown in the Typical Performance Characteristics. This raises the gain-bandwidth product of the voltage loop, resulting in a much more rapid voltage loop response to such perturbations than would occur with a conventional linear gain characteristics.

The Voltage Loop Gain (S)

$$= \frac{\Delta V_{OUT}}{\Delta V_{EAO}} * \frac{\Delta V_{FB}}{\Delta V_{OUT}} * \frac{\Delta V_{EAO}}{\Delta V_{FB}}$$
$$\approx \frac{P_{IN} * 2.5V}{V_{OUTDC}^2 * \Delta V_{EAO} * S * C_{DC}} * GM_V * Z_{CV}$$

Z_{CV}: Compensation Net Work for the Voltage Loop
GMv: Transconductance of VEAO
P_{IN}: Average PFC Input Power
V_{OUTDC}: PFC Boost Output Voltage; typical designed value is 380V.
C_{DC}: PFC Boost Output Capacitor

PFC Current Loop

The current transcondutance amplifier, GMi, I_{EAO} compensation is similar to that of the voltage error amplifier, V_{EAO} with exception of the choice of crossover frequency. The crossover frequency of the
current amplifier should be at least 10 times that of
the voltage amplifier, to prevent interaction with the voltage loop. It should also be limited to less than 1/6th that of the switching frequency, e.g. 8.33kHz for a 50kHz switching frequency.

The Current Loop Gain (S)

$$= \frac{\Delta V_{ISENSE}}{\Delta D_{OFF}} * \frac{\Delta D_{OFF}}{\Delta I_{EAO}} * \frac{\Delta I_{EAO}}{\Delta I_{SENSE}}$$
$$\approx \frac{V_{OUTDC} * R_S}{S * L * 2.5V} * GM_I * Z_{CI}$$

Z_{CI}: Compensation Net Work for the Current Loop
GM_I: Transconductance of IEAO
V_{OUTDC}: PFC Boost Output Voltage; typical designed value is 380V and we use the worst condition to calculate the Z_{CI}
R_{SENSE}: The Sensing Resistor of the Boost Converter
2.5V: The Amplitude of the PFC Leading Edge Modulation Ramp(typical)
L: The Boost Inductor

The gain vs. input voltage of the CM6500UN's voltage error amplifier, V_{EAO} has a specially shaped non-linearity such that under steady-state operating conditions the transconductance of the error amplifier, GMv is at a local minimum. Rapid perturbation in line or load conditions will cause the input to the voltage error amplifier (V_{FB}) to
I_{SENSE} Filter, the RC filter between R_{SENSE} and I_{SENSE} :

There are 2 purposes to add a filter at I_{SENSE} pin:

1.) Protection: During start up or inrush current conditions, it will have a large voltage cross Rs which is the sensing resistor of the PFC boost converter. It requires the I_{SENSE} Filter to attenuate the energy.

2.) To reduce L, the Boost Inductor: The I_{SENSE} Filter To reduce L, the Boost Inductor: The I_{SENSE} Filter also can reduce the Boost Inductor value since the I_{SENSE} Filter behaves like an integrator before going I_{SENSE} which is the input of the current error amplifier, IEAO.

The I_{SENSE} Filter is a RC filter. The resistor value of the I_{SENSE} Filter is 50 ohm because I_{OFFSET} x the resistor can generate an offset voltage of IEAO. By selecting R_{FILTER} equal to 50ohm will keep the offset of the IEAO less than 10mV. Usually, we design the pole of I_{SENSE} Filter at fpfc/6~fpfc=8.33Khz, one sixth of the PFC switching frequency. Therefore, the boost inductor can be reduced 6 times without disturbing the stability. Therefore, the capacitor of the I_{SENSE} Filter, C_{FILTER}, will be around 382.1nF.

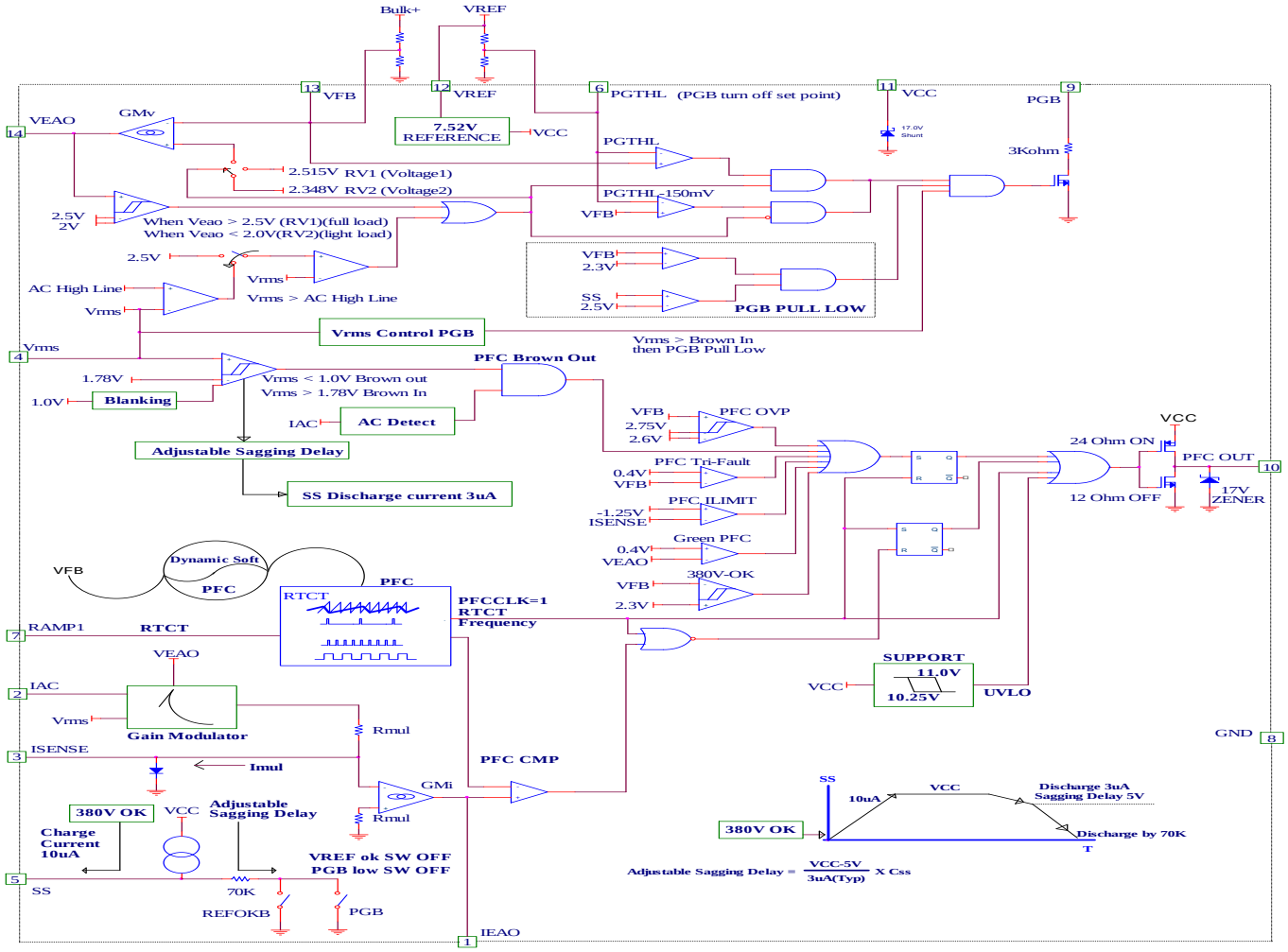


Figure 1. PFC Section Block Diagram

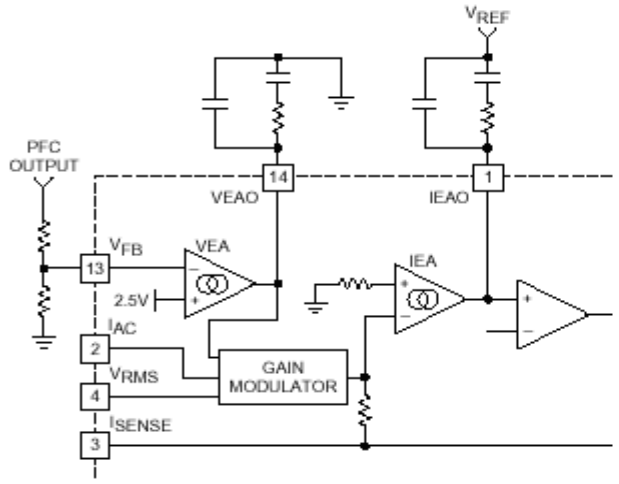


Figure 2. Compensation Network Connections for the Voltage and Current Error Amplifiers

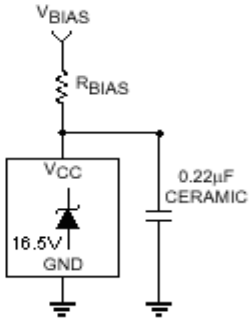


Figure 3. External Component Connections to V_{CC}

Oscillator (RAMP1, or called RTCT)

In CM6500UN, fRTCT = fpfc fRTCT =68Khz, when VEAO=0V, it provides the best performance in the PC application.
The oscillator frequency, fRTCT is the similar formula in CM6800:

$$fRTCT = \frac{1}{t_{RAMP} + t_{DEADTIME}}$$

The dead time of the oscillator is derived from the following equation:

$$t_{RAMP} = C_T \times R_T \times \ln \frac{V_{REF} - 0.78}{V_{REF} - 3.7}$$

at VREF = 7.52V:

$$t_{RAMP} = C_T \times R_T \times 0.5678$$

The dead time of the oscillator may be determined using:

$$t_{DEADTIME} = \frac{2.92V}{10.0mA} \times C_T = 292 \times C_T$$

The dead time is so small ($t_{RAMP} >> t_{DEADTIME}$) that the operating frequency can typically be approximately by:

$$fRTCT = \frac{1}{t_{RAMP}}$$

Ct should be greater than 470pF.

Let us use 1000PF Solving for R_T yields 27K. Selecting standard components values, C_T = 1000pF, and R_T = 27kΩ

The dead time of the oscillator determined PFC minimum off time which is the dead time.

Soft Start (ISS)

There is a ~ 10uA to charge ISS pin. The PFC-soft-start function is implemented with ISS pin.

After PFC Brown Out condition is removed (Vrms is greater than 1.75V.), ISS potential will be raised by the 10uA charge current. ISS potential also determines the VFB threshold until ISS is greater than 2.5V. Therefore, before ISS reaching 2.5V, PFC bulk output voltage is determined by ISS potential until ISS reaching 2.5V.

Generating V_{CC}

After turning on CM6500UN at 11V, the operating voltage can vary from 10V to 21V. That's the two ways to generate VCC. One way is to use auxiliary power supply around 15V, and the other way is to use bootstrap winding to self-bias CM6500UN system. The bootstrap winding can be either taped from PFC boost choke or from the transformer of the DC to DC stage. The ratio of winding transformer for the bootstrap should be set between 18V and 15V.

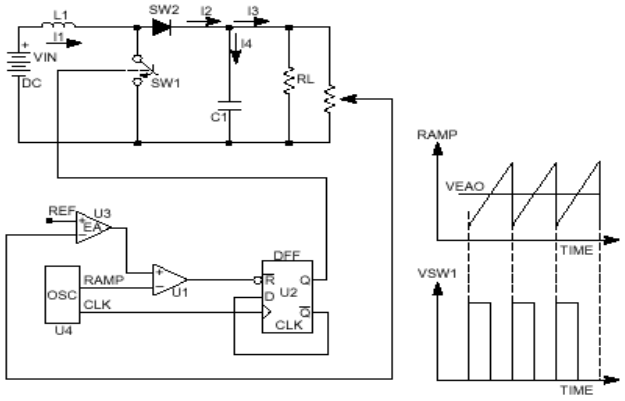


Figure 4. Typical Trailing Edge Control Scheme

In case of leading edge modulation, the switch is turned OFF right at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned ON. The effective duty-cycle of the leading edge modulation is determined during OFF time of the switch.

Figure 5 shows a leading edge control scheme.
One of the advantages of this control technique is that it required only one system clock. Switch 1(SW1) turns off and switch 2 (SW2) turns on at the same instant to minimize the momentary "no-load" period, thus lowering ripple voltage generated by the switching action. With such synchronized switching, the ripple voltage of the first stage is reduced. Calculation and evaluation have shown that the 120Hz component of the PFC's output ripple voltage can be reduced by as much as 30% using this method.

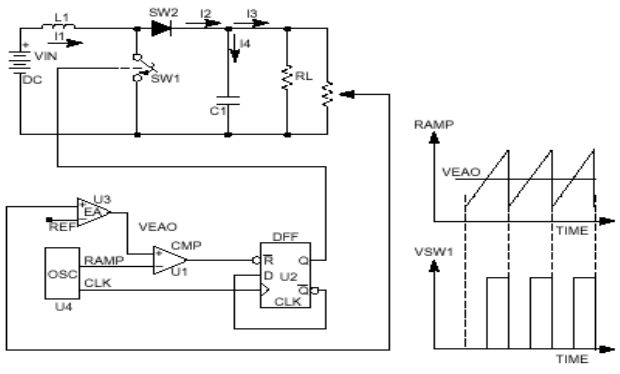


Figure 5. Typical Leading Edge Control Scheme

A filter network is recommended between VCC (pin 11) and bootstrap winding. The resistor of the filter can be set as following.
R_{FILTER} x I_{VCC} ~ 2V, $I_{VCC} = I_{OP} + (Q_{PFCFET} + Q_{PWMFET}) \times fsw$
I_{OP} = 2.1mA (typ.)

If anything goes wrong, and VCC goes beyond 19.4V, the PFC gate (pin 10) drive goes low remains function. The resistor's value must be chosen to meet the operating current requirement of the CM6500UN itself (5mA, max.) plus the current required by the two gate driver outputs.

EXAMPLE:
With a wanting voltage called, V_{BIAS} ,of 18V, a VCC of 15V and the CM6500UN driving a total gate charge of 90nC at 100kHz (e.g. 1 IRF840 MOSFET and 2 IRF820 MOSFET), the gate driver current required is:

$$I_{GATEDRIVE} = 100kHz \times 90nC = 9mA$$

$$R_{BIAS} = \frac{V_{BIAS} - V_{CC}}{I_{CC} + I_G}$$

$$R_{BIAS} = \frac{18V - 15V}{5mA + 9mA}$$

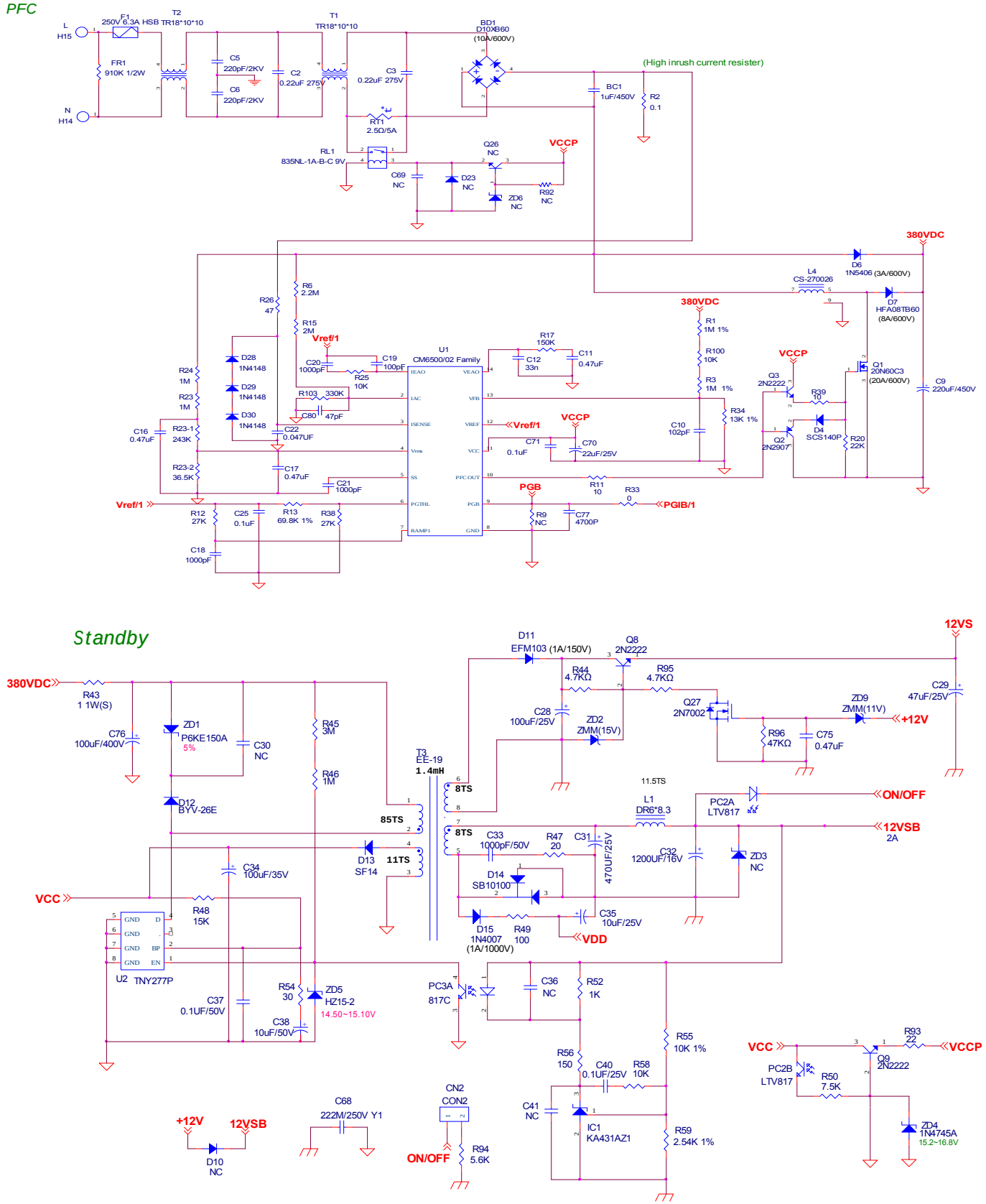
Choose R_{BIAS} = 214Ω

The CM6500UN should be locally bypassed with a 1.0 μF ceramic capacitor. In most applications, an electrolytic capacitor of between 47 μF and 220 μF is also required across the part, both for filtering and as part of the start-up bootstrap circuitry.

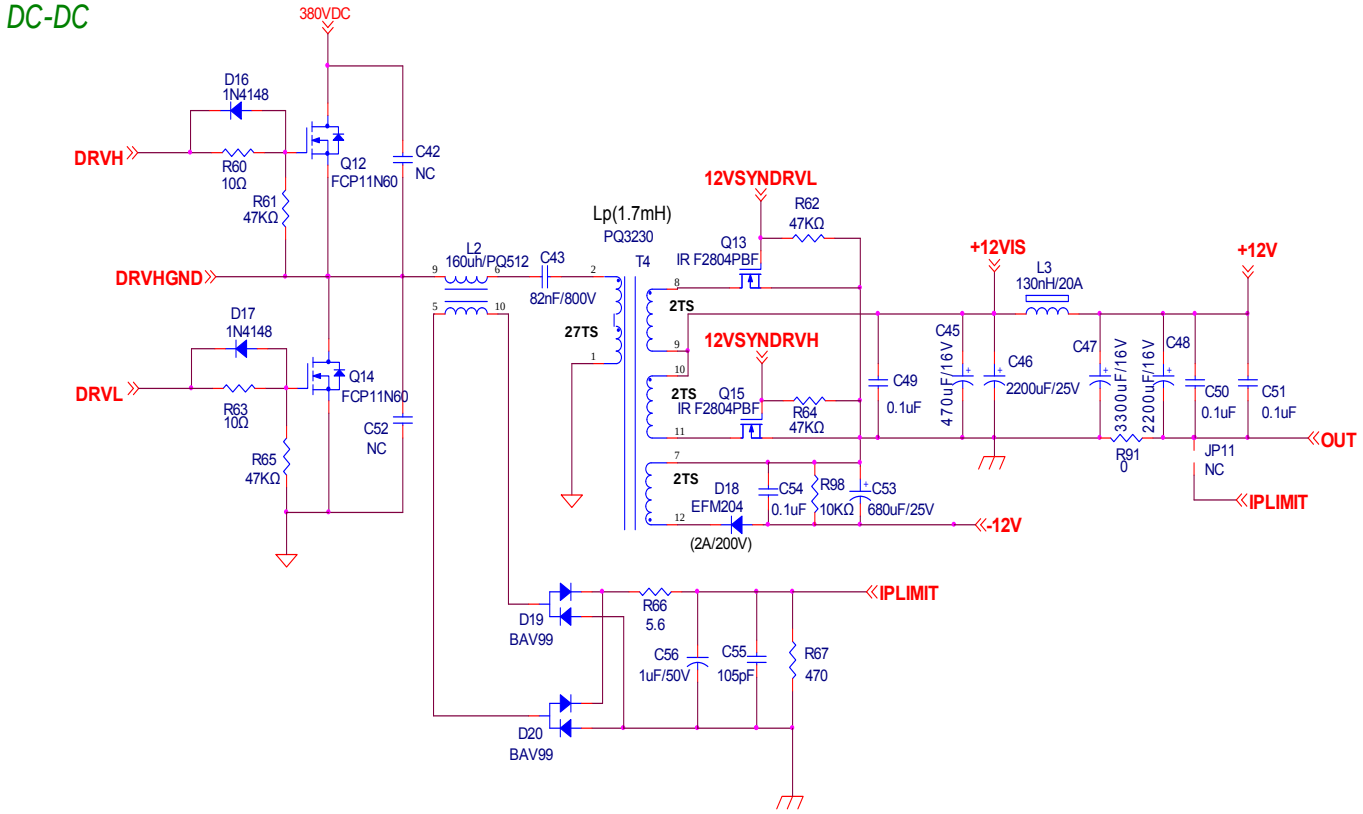
Leading/Trailing Modulation

Conventional Pulse Width Modulation (PWM) techniques employ trailing edge modulation in which the switch will turn on right after the trailing edge of the system clock. The error amplifier output is then compared with the modulating ramp up. The effective duty cycle of the trailing edge modulation is determined during the ON time of the switch. Figure 4 shows a typical trailing edge control scheme.

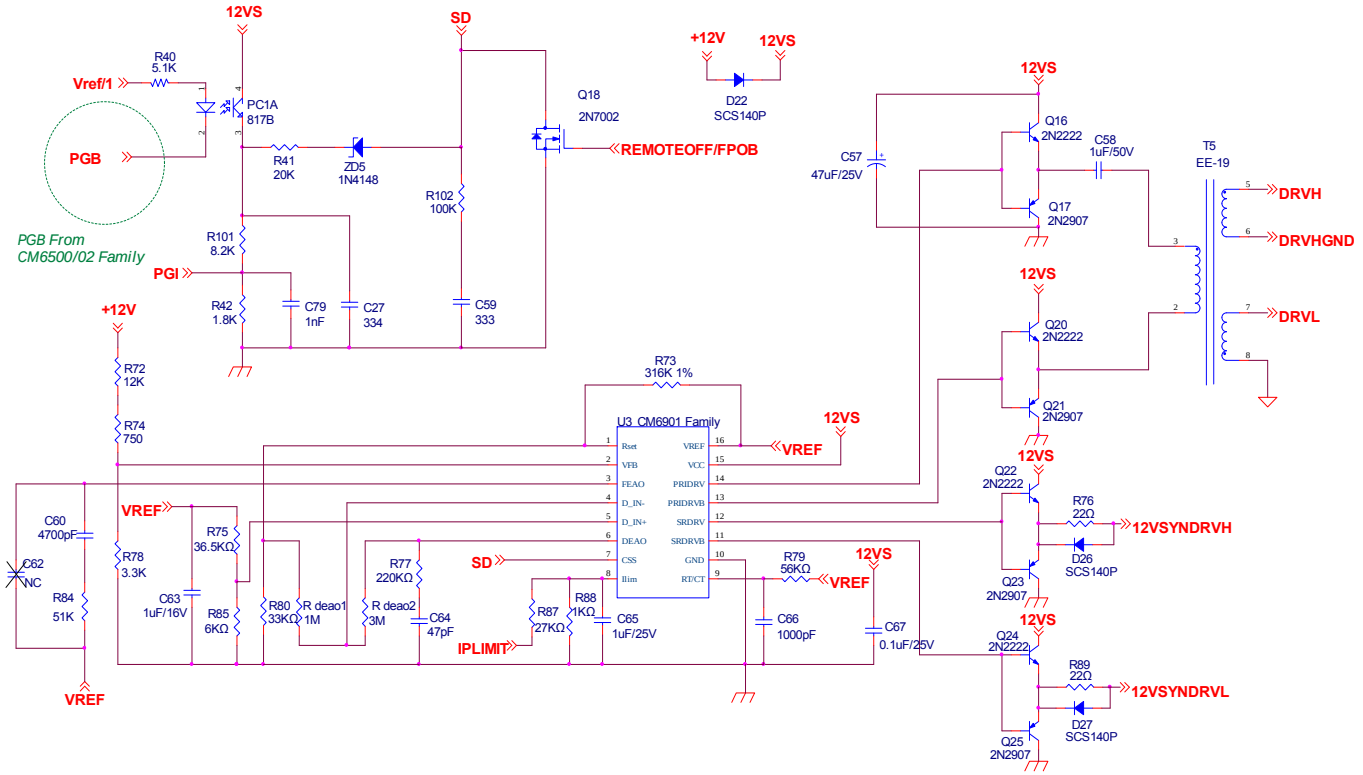
TYPICAL APPLCATION CIRCUIT



DC-DC

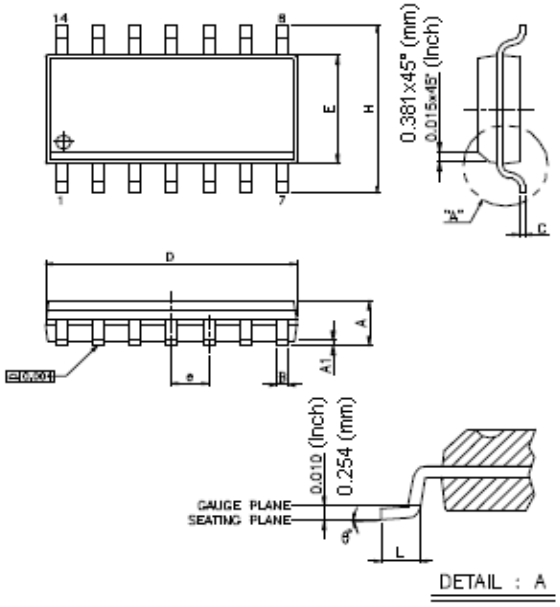


SLS Controller



PACKAGE DIMENSION

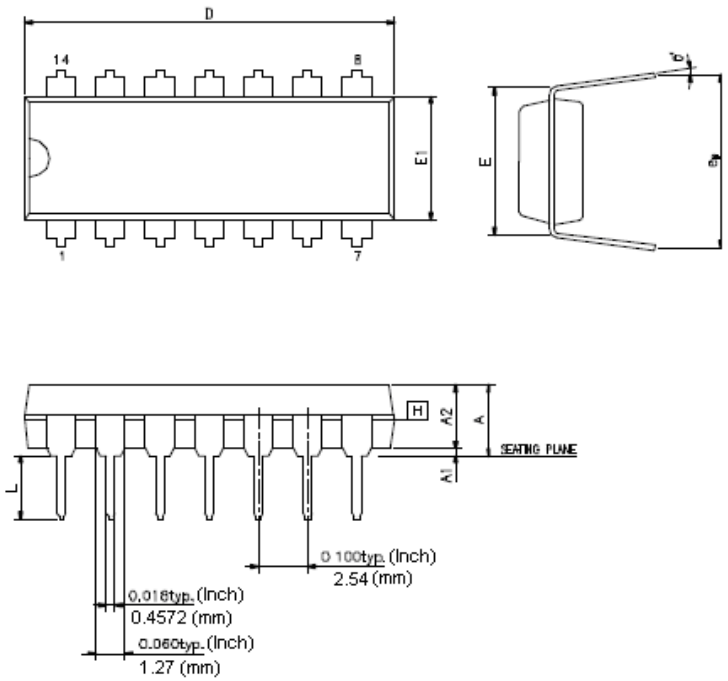
14-PIN SOP (S14)



Items	Spec (Inch)			Items	Spec (Millimeters)		
	Min	Nom	Max		Min	Nom	Max
A	0.058	0.064	0.068	A	1.4732	1.6256	1.7272
A1	0.004	----	0.01	A1	0.1016	----	0.254
B	0.013	0.016	0.02	B	0.3302	0.4064	0.508
C	0.0075	0.008	0.0098	C	0.1905	0.2032	0.2489
D	0.336	0.341	0.344	D	8.5344	8.6614	8.7376
E	0.15	0.154	0.157	E	3.81	3.9116	3.9878
e	----	0.05	----	e	----	1.27	----
H	0.228	0.236	0.244	H	5.7912	5.9944	6.1976
L	0.015	0.025	0.05	L	0.381	0.635	1.27
θ°	0°	----	8°	θ°	0°	----	8°

NOTES:
1.JEDEC OUTLINE : MS-012 AB
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.005in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

14-PIN DIP (P14)



SYMBOLS	SPEC (Inch)			SPEC (Millimeters)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-----	-----	0.21	-----	-----	5.334
A1	0.015	-----	-----	0.381	-----	-----
A2	0.125	0.13	0.135	3.175	3.302	3.429
D	0.735	0.75	0.775	18.67	19.05	19.69
E	0.3 BSC.			7.62 BSC.		
E1	0.245	0.25	0.255	6.223	6.35	6.477
L	0.115	0.13	0.15	2.921	3.302	3.81
eB	0.335	0.355	0.375	8.509	9.017	9.525
θ°	0	7	15	0	7	15

NOTES:
1.JEDEC OUTLINE : MS-001 AA
2."D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3.eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4.POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5.DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM.
6.DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY

IMPORTANT NOTICE

Champion Microelectronic Corporation (CMC) reserves the right to make changes to its products or to discontinue any integrated circuit product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

A few applications using integrated circuit products may involve potential risks of death, personal injury, or severe property or environmental damage. CMC integrated circuit products are not designed, intended, authorized, or warranted to be suitable for use in life-support applications, devices or systems or other critical applications. Use of CMC products in such applications is understood to be fully at the risk of the customer. In order to minimize risks associated with the customer's applications, the customer should provide adequate design and operating safeguards.

HsinChu Headquarter

5F, No. 11, Park Avenue II,
Science-Based Industrial Park,
HsinChu City, Taiwan

TEL: +886-3-567 9979
FAX: +886-3-567 9909
http://www.champion-micro.com

Sales & Marketing

21F., No. 96, Sec. 1, Sintai 5th Rd., Sijhih City,
Taipei County 22102,
Taiwan, R.O.C.

TEL: +886-2-2696 3558
FAX: +886-2-2696 3559